ABSTRACT OF THE DISCLOSURE

A digital switching system comprises multiplexing means for multiplexing time slots from a plurality of circuits, multiplexed respectively, by the multiplexed time slot unit, switching memory means for storing and switching data of the time slots supplied from the multiplexing means, for one frame portion, switching control means comprising switching correspondence means for directing interchange of the time slots of the switching memory means in response to a switching request from an upper layer controller, and demultiplexing means for demultiplexing data as read out using data supplied from the switching correspondence means as addresses of the switching memory means into the plurality of the circuits, the switching correspondence means further comprising information receiving means for receiving connection information from the upper layer controller, read-out regulating means for writing the connection information received through the information receiving means to an address designated by the connection information, in a first memory means and a second memory means, respectively, for storing the connection information corresponding to before or after switching, and sequentially reading out the connection information stored, in read-out order of the switching memory means, network switching control means for generating a switching signal in synchronization with an internal standard timing in response to a switching directive of a network, delivered from the upper layer controller, and

read-out selection means for selecting read-out from either the first memory means of the read-out regulating means or the second memory means of the same in response to the switching signal delivered from the network switching control means.